Claims

1. A signal-processing unit comprising:

an input line that is provided with a plurality of analog input signal lines;

a multiplexer circuit that transmits said plurality of analog signals from said input line to one signal line in the subsequent stage in a desired sequence;

an analog-digital conversion circuit that converts an analog signal into a digital signal and outputs it; and

a cross talk compensation circuit that with respect to each of a plurality of signals having been synchronously inputted to a signal-processing unit out of signals having been sequentially outputted from said analog-digital conversion circuit, a coefficient of an effect level between each of a plurality of signals and the other plural signals interfering with each other is calculated one-by one, and data obtained by multiplying the signals by said coefficients are added up.

2. The signal-processing unit according to claim 1, characterized in that a cross talk compensation circuit comprises: a counter that counts the number of parallel signals of data input; a shift register that consists of a plurality of storage blocks, and that shifts said data input to the subsequent stage based on a clock period; a signal hold circuit that holds data until all signals are stored in said storage block; a multiplier that multiplies each data held in said signal hold circuit by coefficient data having been preliminarily obtained by the calculation of a signal interference level between the signals; and

an adder that adds up respective signals of said multiplier and outputs an output data of which cross talk has been compensated.

3. A signal-processing unit characterized by comprising:

an input line provided with a plurality of analog input signal lines;

a multiplexer circuit that transmits said plurality of analog signals from said input line into one signal line in the subsequent stage in a desired sequence;

an analog-digital conversion circuit that converts an analog signal into a digital signal and outputs it; and

a cross talk compensation circuit that with respect to one signal out of signals having been sequentially outputted from said analog-digital conversion circuit, a coefficient of an effect level between a plurality of signals before and after said signal and a plurality of signals interfering with each other is calculated, and data obtained by multiplying the signals by said coefficients are added up.

4. The signal-processing unit according to claim 3, characterized in that a cross talk compensation circuit comprises: a counter that counts the number of parallel signals of data input; a shift register that consists of a plurality of storage blocks, and that shifts said data input to the subsequent stage based on a clock period; a multiplier that multiplies each data held in each of said storage blocks by coefficient data having been

preliminarily obtained by the calculation of a signal interference level between the signals; and an adder that adds up respective signals of said multiplier and outputs an output data of which cross talk has been compensated.

5. The signal-processing unit according to claim 1 or 3, characterized by being provided with a communication processing circuit that alters a cross talk elimination coefficient to be stored in said storage device from outside the device.